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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/659,918

09/11/2003

Jason H. Anderson

X-1396 US

6014

24309

7590

04/06/2005

XILINX, INC  
ATTN: LEGAL DEPARTMENT  
2100 LOGIC DR  
SAN JOSE, CA 95124

EXAMINER

SIEK, VUTHE

ART UNIT

PAPER NUMBER

2825

DATE MAILED: 04/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/659,918

Applicant(s)

ANDERSON ET AL.

Examiner

Vuthe Siek

Art Unit

2825

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 11 September 2003.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-25 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-25 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 11 September 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 9/11/03; 6/28/04.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

### **DETAILED ACTION**

1. This office action is in response to application 10/659,918 filed on 9/11/2003.

Claims 1-25 remain pending in the application.

#### ***Claim Objections***

2. Claims 3-4 are objected to because of the following informalities: the claimed limitations in both claims are confused, since the range from 1 to 0.5 and 0.5 to 1 belonged to the same high power range. Appropriate correction is required.

#### ***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 16 and 22 are rejected under 35 U.S.C. 102(b) as being anticipated by Khouja et al. (6,345,379).
5. As to claims 1, 16 and 22, Khouja et al. teach a method and apparatus for estimating internal power consumption of an electronic circuit system represented as netlist including optimizing leakage power in the system comprising determining a static probability of a signal in the system and if the static probability is in a high power range, then modifying the signal such that static probability of the modified signal is in a low power range (for example Khouja et al. teach computing toggle rates, static probability at a point in a net is an estimate of the total fraction of time that the node spends at the

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logic value of one, the method takes static probability values and toggle rates for every primary input and estimates the toggle values at the internal nodes and outputs from the values at the primary inputs), and such that functionality of the system is not affected (Fig. 4-5, col. 4 line 40-67, col. 5, line 10 to col. 6 line 64; col. 10 line 15 to col. 21, col. 37, 46-48 summary).

***Claim Rejections - 35 USC § 103***

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 2-15, 17-21 and 23-25 are rejected under 35 U.S.C. 103(a) as being obvious over Khouja et al. (6,345,379).

8. As to claims 2-7, 17-18 and 23, Khouja et al. teach the signal is a digital signal (logic 0 and 1) and modifying the signal comprising inverting the signal (toggle signal); the low power range is a range from 0 to 0.5 and the high power range is a range from 0.5 to 1 (they are art inherent of the characteristics of a digital signal of logic 0 and 1); wherein inverting the signal comprising inverting an output of a source of the signal and inverting an input of a sink of the signal (toggle signal); inverting the output of the source comprising adding an inverter at the output of the source (toggle signal meaning that placing inverter that must invert a signal state from 0 to 1 and vice versa); inverting the

input of the sink comprising adding an inverter at the input of the sink (toggle signal meaning that placing inverter that must invert a signal state from 0 to 1 and vice versa).

9. As to claims 8-10, 19-21 and 24-25, Khouja et al. teach optimizing a leakage power of a digital circuit. It is well known to one ordinary skill in the art that a programmable logic device is a circuit beyond the scope to the teachings of Khouja et al. It is well known in the art that a programmable logic device includes a lookup table. Khouja et al. teach inverting the signal by toggling a signal; therefore the inverting the signal has no area or performance penalty. Khouja et al. also teach an example of a digital circuit including a memory element therefore the inverting the output of the source including inverting each bit of the lookup table by toggling a signal and inverting the output of the sink comprising permuting the lookup table memory contents such that the lookup table expects an inverted input (same meaning of toggle signals in order to reduce a leakage power of the memory element) (Fig. 26).

10. As to claim 11, Khouja et al. teach biasing the static probability by modifying the system such that the static probability is closer to the low power range (toggle signal from high power range to low power range) (col. 13-14).

11. As to claims 12-15, Khouja et al. toggle signal on nets where the nets connected from a source to a sink (Examples shown in Fig. 10, 12, at least see col. 13-14). In order to reduce a low leakage power, transitions of signals or toggle signals must faster enough in the nets, therefore it would have been obvious to one ordinary skill in art to place a source of the signal physically close to a sink of the signal, where the placing including assigning a high priority to the signal in a place and route operation, the

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routing the signal in a manner that minimizes an objective function related to leakage power consumed in the routing circuits (nets) in order to shortening the nets to thereby shortening transition time of signals or toggle signals.

12. Claims 1, 16, and 22 are rejected under 35 U.S.C. 102(b) as being anticipated by Cohn et al. (6,687,883).

13. As to claims 1, 16 and 22, Cohn et al. teach a method and apparatus for estimating internal power consumption of an electronic circuit system represented as netlist including optimizing leakage power in the system comprising determining a static probability of a signal in the system and if the static probability is in a high power range, then modifying the signal such that static probability of the modified signal is in a low power range, and such that functionality of the system is not affected (Forcing a logic state from one logic state 1 to logic 0 and vice versa in order to minimize a leakage power of the circuit; the forcing of logic state to change from one logic state to another logic state is done by modifying a network without affecting function of the circuit or by inverting a logic state signal; col. 7, line 65-67, col. 8, lines 20-37; col. 10, lines 19-67, col. 11, lines 1-34; col. 11, lines 59-67; col. 12, lines 1-67; col. 15, lines 2-44; col. 16, lines 33-53; col. 18, lines 1-50). Note that a logic 1 state and logic 0 state are obtained by applying a power supply within a power supply range.

### ***Claim Rejections - 35 USC § 103***

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

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(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

15. Claims 2-15, 17-21 and 23-25 are rejected under 35 U.S.C. 103(a) as being obvious over Cohn et al. (6,687,883).

16. As to claims 2-7, 17-18 and 23, Cohn et al. teach the signal is a digital signal (logic 0 and 1) and modifying the signal comprising inverting the signal (col. 8, col. 15, col. 18; the low power range is a range from 0 to 0.5 and the high power range is a range from 0.5 to 1 (they are art inherent of the characteristics of a digital signal of logic 0 and 1 using a low power supply); wherein inverting the signal comprising inverting an output of a source of the signal and inverting an input of a sink of the signal (toggle signal); inverting the output of the source comprising adding an inverter at the output of the source (inverting signal by an inverter); inverting the input of the sink comprising adding an inverter at the input of the sink (col. 8, lines 20-38; col. 11-12; col. 15, col. 16, col. 18).

17. As to claims 8-10, 19-21 and 24-25, Cohn et al. teach optimizing a leakage power of a digital circuit. It is well known to one ordinary skill in the art that a programmable logic device is a circuit beyond the scope to the teachings of Cohn et al. It is well known in the art that a programmable logic device includes a lookup table. Cohn et al. teach inverting the signal by toggling a signal, ;herefore the inverting the signal has no area or performance penalty. Cohn et al. also teach an example of a digital circuit including a memory element therefore the inverting the output of the

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source including inverting each bit of the lookup table by toggling a signal and inverting the output of the sink comprising permuting the lookup table memory contents such that the lookup table expects an inverted input (col. 7, line 65-67, col. 8, lines 20-37; col. 10, lines 19-67, col. 11, lines 1-34; col. 11, lines 59-67; col. 12, lines 1-67; col. 15, lines 2-44; col. 16, lines 33-53; col. 18, lines 1-50).

18. As to claim 11, Cohn et al. teach biasing the static probability by modifying the system such that the static probability is closer to the low power range (col. 7, line 65-67, col. 8, lines 20-37; col. 10, lines 19-67, col. 11, lines 1-34; col. 11, lines 59-67; col. 12, lines 1-67; col. 15, lines 2-44; col. 16, lines 33-53; col. 18, lines 1-50).

19. As to claims 12-15, Cohn et al. teach a circuit placement and routing in order to minimizing a leakage power of the circuit (Fig. 2-5, 8).

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***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vuthe Siek whose telephone number is (571) 272-1906. The examiner can normally be reached on Increase Flextime.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vuthe Siek

  
**VUTHE SIEK**  
**PRIMARY EXAMINER**